COURSE CODE	COURSE TITLE	L	T	P	C
1153CS101	BASIC COMPUTER SYSTEM ORGANIZATION AND ARCHITECTURE	3	0	0	3

Course Category: Allied Elective

A. Preamble:

This course provides the basics of organizational and architectural issues of a digital computer analyze performance issues in processor and memory design of a digital computer, various data transfer techniques in digital and performance improvement using instruction level parallelism.

B. Prerequisite Courses:

Sl. No	Course Code	Course Name
1	1150CS201	Problem Solving using C

C. Related Courses:

Sl. No	Course Code	Course Name
		Nil

D. Course Educational Objectives:

Learners are exposed to

- Hardware-software interface.
- Arithmetic and logic unit, fixed point and floating-point arithmetic operations.
- The concept of pipelining.
- Hierarchical memory system including cache memories and virtual memory.
- Different ways of communicating with I/O devices and standard I/O interfaces.\

E. Course Outcomes:

Upon the successful completion of the course, students will be able to:

CO Nos.	Course Outcomes	Level of learning domain (Based on revised Bloom's)
CO1	Explain about the basics, instruction set and addressing modes of a computer.	K2
CO2	Familiarize in the arithmetic operations.	K2
CO3	Design and analyze concept of pipeline for consistent execution of instructions with hazards.	K2
CO4	Explain the concepts of Instruction Level parallelism.	K2
CO5	Demonstrate knowledge about state-of-the-art I/O, memory and storage systems	K3

F. Correlation of COs with POs:

Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	**M**												**L**		
CO2	**L**	**M**										**M**	**H**		
CO3	**M**	**M**		**M**								**L**		**L**	**M**
CO4	**M**	**M**		**M**								**L**		**L**	**L**
CO5	**M**	**M**											**M**		**L**

H- Strong; M-Medium; L-Low

G. Course Content:

UNIT I OVERVIEW& INSTRUCTIONS 9

Eight ideas – Components of a computer system – Technology – Performance – Power wall – Uniprocessors to multiprocessors; Instructions – operations and operands – representing instructions –Addressing and addressing modes.

UNIT II ARITHMETIC OPERATIONS 8

ALU - Addition and subtraction – Multiplication – Division – Floating Point operations.

UNIT III PROCESSOR AND CONTROL UNIT 10

Basic MIPS implementation – Building datapath –Pipelining – Pipelined datapath and control – Handling Data hazards & Control hazards – Exceptions.

UNIT IV PARALLELISM 9

Instruction-level-parallelism – Parallel processing challenges – Flynn's classification – Hardware multithreading – Multicore processors.

UNIT V MEMORY AND I/O SYSTEMS 9

Memory hierarchy - Memory technologies – Cache basics –Cache Memory Mapping Techniques– Measuring and improving cache performance - Virtual memory, TLBs, Page Replacement Techniques- Input/output system- DMA and interrupts, I/O processors.

Total: 45 Hours

H. Learning Resources

i.Text Books:

1. David A. Patterson and John L. Hennessy, "Computer Organization and Design: The Hardware/Software interface", Fourth Edition, Elsevier, 2011.
2. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Fifth Edition, Tata McGraw Hill, 2002.

Reference Books:

1 M.Morris Mano, "Computer System Architecture"- Third Edition, Pearson Education, 2007.

2.Behrooz Parhami, "Computer Architecture", Oxford University Press, 2007.

3. V.P. Heuring, H.F. Jordan, "Computer Systems Design and Architecture", Second Edition, Pearson Education, 2004.

4, William Stallings, "Computer Organization and Architecture – Designing for Performance", Sixth Edition, Pearson Education, 2003.

5. John P. Hayes, "Computer Architecture and Organization", Third Edition, Tata McGraw Hill, 1998.

iii. Online Resources:

1. www.Computer Architecture Home Page
2. ACM Special Interest Group on Computer
3. IEEE Technical Committee on Computer Architecture
4. williamstallings.com/Computer Organization/COA8e-Instructor/