

Laboratory Name: Vel Tech- Chips to Startup (C2S) Centre of Excellence

Venue: 1412

Laboratory In-Charge: Dr. S.Shiyamala , Professor, Chief Investigator

Dr.J.L.Mazher Iqbal, Professor, Co-Chief Investigator

TECHNICAL MANPOWER

Laboratory Assistant: Ms.M.Suriya

Qualification:MCA

LABORATORY SPACE AND STUDENT ALLOCATION

Area of the Laboratory : 60sq.m

No. of students per session : 30

Batch Size : Single

Weekly Utilization Status : Open Access for
Research & Development Activities

DESCRIPTION ABOUT THE LABORATORY

- The Vel Tech – Chips to Startup (C2S) Centre of Excellence is an advanced semiconductor design laboratory supported by MeitY, Government of India
- Provides access to industry-standard EDA tools for VLSI design, simulation, verification, and fabrication workflows.
- Equipped with leading tools including Synopsys, Cadence, Siemens EDA, AMD Xilinx, ANSYS, and Silvaco.
- Enables hands-on experience in IC design, simulation, verification, and device-level analysis.
- Supports learning and research in Analog & Digital design, physical design, and system-level verification.

COST OF THE LABORATORY

MeitY Sponsored ₹10 Crore worth EDA Tools and Renesas Development Boards

OBJECTIVES

- Hands-on VLSI design using industry tools
- Promote research in semiconductor technologies
- Skill development aligned with chip design industry
- Promote innovation leading to publications & patents

KEY ACTIVITIES

- VACs, Workshops & FDPs
- Hands-on EDA Tool Training
- VLSI & Embedded Projects
- Hackathons & Design Challenges

PHD SCHOLARS & RESEARCH FOCUS

Doctoral Research Areas

- CMOS & Nanoscale Devices
- Analog, Digital & Mixed Signal VLSI
- TCAD & Device Modeling
- Low-Power & High-Speed Design
- FPGA, SoC & Embedded Systems
- AI Hardware & VLSI Security

STUDENT BENEFITS

- Hands-on Industry Tool Exposure
- Internship Opportunities
- Certification Programs
- Real-time Project Experience
- Placement Support

Scan for Training / Lab Access Registration



LIST OF SPONSORED EDA & INDUSTRY TOOLS



Renesas Development Board (MeitY Sponsored)

**“Empowering Future Semiconductor Engineers
through Industry-Driven Learning”**