COURSE CODE: **1152EE122**	COURSE TITLE: **VLSI SYSTEM & DESIGN**	L	T	P	C
		3	**0**	**0**	**3**

COURSE CATEGORY:

Program Elective

PREAMBLE :

This course provides an introduction to the design and implementation of VLSI circuits for complex digital systems and the focus is on CMOS technology. In this course, students will get exposure to the fundamental concepts and structures of designing digital VLSI systems that include CMOS devices and circuits, standard CMOS fabrication processes, CMOS design rules, static and dynamic logic structures, interconnect analysis, CMOS chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture & VHDL

PREREQUISITE COURSES:

- Analog Electronics-I

RELATED COURSES:

- Application Specific Integrated circuits

COURSE EDUCATIONAL OBJECTIVES:

The objectives of the course are to make the students,

- The basic CMOS circuits and allied process technology
- The techniques of chip design using programmable devices.
- The CMOS testing
- The concepts of designing VLSI subsystems
- The concepts of modelling a digital system using Hardware Description Language.

COURSE OUTCOMES :

Upon the successful completion of the course, students will be able to:

CO Nos.	Course Outcomes	Level of learning domain (Based on revised Bloom's taxonomy)
C01	Describe CMOS Technology	K2
C02	Describe CMOS Chip Design Techniques.	K2
C03	Explain the CMOS testing.	K2
C04	Describe the digital design using Programmable logic devices	K2
C05	Design the digital circuits using Verilog, a Hardware Description Language	K3

CORRELATION OF COs AND POs

COs	PROGRAM OUTCOMES											
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	L		H								M	
CO2			M					M			L	
CO3	M		M								M	
CO4			H					M			M	
CO5			M									

COURSE CONTENT:

UNIT I	**CMOS TECHNOLOGY**	**9**

An Overview of silicon semiconductor technology, Basic CMOS technology: n Well, P Well, Twin Tub and SOI process. Circuit Elements : Resistors, Capacitors, EAROM. Latch Up and Prevention. Layout Design rules, Stick Diagram, Physical Design : Basic Concepts, CAD tools. Physical Design of logic gates : inverter, NAND, NOR, Design hierarchies.

UNIT II	**CMOS CHIP DESIGN**	**9**

Logic Design with CMOS : MOSFETS as switches, Basic logic gates in CMOS and Complex logic gates. Transmission gates : Muxes and latches. CMOS chip design options : full custom ASIC'S, semi custom ASIC and programmable ASIC. Programmble logic structures : 22V10, programming PAL's, Programmable interconnect Reprogrammable GA : Xilinx programmable GA, Features and internal structure of CPLDs, FPGAs, designing with CPLDs and FPGAs. Introduction to IC floor planning and testing, ASIC Design flow.

UNIT III	**CMOS TESTING**	**9**

Need for testing , manufacturing test principles, Design strategies for test : design for testability, combinational logic testing, sequential logic testing, fault model types, ATPG, Boundary scan test, built in self test, DFT schemes. Chip level and system level test techniques.

UNIT IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**	**9**

EPROM to realize a sequential circuit, Programmable logic devices : ROM, PLA, PAL, PLD and DESIGN, designing a synchronous sequential circuit using a GAL, realization state machine using PLD, FPGA : introduction, Switching matrix , FPGA Xilinx 2000 , Xilinx 3000.

UNIT V	**SPECIFICATION USING VERILOG HDL**	**9**

Basic concepts, language features, VLSI design flow, identifiers, arrays, instances, value set, ports, gate delays.

Types of Verilog description – structural gate level RTL, data flow RTL and structural and behavioral RTL descriptions

structural gate level RTL : Half adder , Full adder , Ripple carry adder, Multiplexer, encoder, decoder, comparator, equality detector, D-latch, D Flip Flop, JK flip flop.

Data flow RTL : Operators, Combinational logic and sequential logic examples.

structural and behavioral RTL : Delays and Timing controls ,Procedural assignments and conditional assignments, Multiplexer, Combinational logic and sequential logic examples.

TOTAL: 45 PERIODS

TEXT BOOKS:

1. Weste & E Shraghian : Principles of CMOS VLSI Design (2 / e) Addison Wesley, 1993 for Unit I to Unit I II.
2. Samir Palnitkar, Verilog HDL – Guide to digital design and synthesis, III edition , Pearson Education, 2003 for Unit V

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