Course Code	Course Title	L	T	P	C
1152EC242	FPGA ARCHITECTURE TECHNOLOGIES AND TOOLS	2	0	2	3

a) Course Category

Program Elective

b) Preamble

This course discusses the features, programming and applications of Programmable Logic Devices. The students shall emphasize the VLSI architectures such as Altera series Max 5000/7000 series, cypress flash, Virtex-II, Flex architectures, case study. It provides VLSI system design experience using FSM. This course introduce the VHDL models, process, concurrent and sequential statements, loops, delay models, library packages, functions, procedures, test bench and Digital Front End Digital Design Tools

c) Prerequisite

VLSI Design

d) Related Courses

Reconfigurable Computing With FPGA

e) Course Outcomes

Upon the successful completion of the course, students will be able to:

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Illustrate the features of Programmable Logic Devices, CPLD, performance and its applications.	K2
CO2	Summarize the various FPGA architectures, programmable interconnects and one hot encoding.	K2
CO3	Explain the VLSI system design experience using FSM.	K2
CO4	Account for the syntax and behavior of the VHDL language	K2
CO5	Explain the Digital Front End Digital Design Tools for FPGAs & ASICs	K2

f)	Correlation of COs with POs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	H	H	M	L	-	-	-	-	-	-	-	H	M	-
CO2	H	L	M	H	-	-	-	-	-	-	-	L	H	-
CO3	M	L	H	M	-	-	-	-	-	-	-	L	L	-
CO4	H	H	M	H	-	-	-	-	-	-	-	M	M	-
CO5	M	M	H	H	-	-	-	-	-	-	-	H	L	-

g) Course Content

UNIT I PROGRAMMABLE LOGIC DEVICE 9

Introduction, ROM, PLD, PLA, PAL, GAL– Features, CPLD- Commercially available CPLD - Altera series – Max 5000/7000 series - Cypres FLASH 370 Device Technology, Lattice LSI's Architectures – 3000 Series –Applications of CPLDs, Speed Performance and in system programmability.

UNIT II FIELD PROGRAMMABLE GATE ARRAYS 9

FPGAs- Logic blocks, Routing architecture, programmable interconnect, Mapping for FPGAs, Xilinx FPGA Architecture: Xilinx XC3000, XC4000 – Altera Architecture: FLEX 8000, One hot encoding, Case studies: Xilinx Virtex II Pro.

UNIT III FINITE STATE MACHINES 9

Top down Approach to Design, State diagram, State Transition Table, State assignments for FPGAs, Case study Mealy & Moore Machines, Pipelining, FSM issues-Starring state, Power on Reset, State diagram optimization, fault Tolerance.

UNIT IV VHDL FOR SYNTHESIS 9

Introduction, data flow, behavioral, structural models, operators, process, concurrent statements, Sequential Statements, Loops, Modeling Delays, Sequential Circuits, FSM Coding, Library, Packages, Functions, Procedures, Test bench.

UNIT V DIGITAL FRONT END DESIGN TOOLS 9

Digital Front End Design Tools for FPGAs & ASICs: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of paraller adder, multiplexers, counters, CMOS design using Mentor graphics Tools.

Total 45 Hrs

h) List of experiments

S. No	Practical Exercises (15 Hours)	COs

1.	Introduction to Software and Hardware Tools	CO1, CO2
2.	CMOS inverter design using Mentor graphics Tools	CO5
3.	Delay Modelling using VHDL	CO4
4.	Implementation of Parallel Adder using VDHL	CO5
5.	Implementation of counters using VHDL	CO3
5.	FSM Coding	CO3

i) Learning Resources

Text Books

1. P.K.Chan& S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. M. J. S. Smith, "Application Specific Integrated Circuits," Addition – Wesley Longman Inc., 1997.
3. VHDL Primer, J. Bhasker, American Telephone and Telegraph Company, Bell Laboratories Division, P T R Prentice Hall, Englewood Cliffs, New Jersey07632
4. Douglas L. Perry, VHDL: Programming by Example, McGraw-Hill Education, Fouth Edition.
5. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer, Academic Publications, 1994.

Reference Books

1. Jon F Wakerly, Digital Design: Principles and Practices, Prentice Hall.
2. Kevin Skahil, VHDL for programmable logic, Addison Wesley.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.