| Course Code | Course Title | L | T | P | C |
|---|---|---|---|---|---|
| 1152EC143 | ARCHITECTURAL DESIGN OF DIGITAL INTEGRATED CIRCUITS | 3 | 0 | 0 | 3 |

**a) Course Category**

Program Elective

**b) Preamble**

This course explains the fundamental principles of algorithms available for performing arithmetic operations on digital computers.

**c) Prerequisite**

Digital Electronics

**d) Related Courses**

Low power VLSI

**e) Course Outcomes**

Upon the successful completion of the course, students will be able to:

| CO Nos. | Course Outcomes | Knowledge Level (Based on Revised Bloom's Taxonomy) |
|---|---|---|
| CO1 | Describe any algorithm to efficient architecture mapping | K2 |
| CO2 | Construct various adder architecture | K2 |
| CO3 | Construct various multiplier architecture | K2 |
| CO4 | Describe CORDIC architecture with any applications | K2 |
| CO5 | Illustrate the timing issues in VLSI | K2 |

| f) | Correlation of COs with POs | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
| CO1 | H | H | M | L | M | | | | | | | H | M | |
| CO2 | H | L | M | H | L | | | | | | | L | H | |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO3** | M | L | H | M | | M | L | | | | | L | L | |
| **CO4** | H | H | M | H | L | | | | | | | M | M | |
| **CO5** | M | M | H | H | L | | | | | | | H | L | |

**g) Course Content**

**UNIT I ALGORITHM TO EFFICIENT ARCHITECTURE MAPPING 9**

One bit incrementer, four bit incrementer, n-bit incrementer, ones' complement, two's complement, sum of N –natural numbers, prioritization, greatest common divisor (GCD).

**UNIT II ADDER ARCHITECTURE 9**

Single bit addition, Carry – Ripple adder, Carry – Skip adder, Carry-Lookahead adder, Carry –Select adder, Carry – Increment adder, Tree adder.

**UNIT III MULTIPLIERARCHITECTURE 9**

Tree multiplication, Array multiplication, signed multi-operand addition, squaring, shift and add multiplier, synchronous shift and add multiplier, Booth algorithm.

**UNIT IV CORDIC ARCHITECTURE 9**

CORDIC method, rotation and vectoring mode, convergence, precision and range, scaling factor and compensation, implementations: word-serial and pipelined, New techniques – Micro rotation to Angel Recoding (MAR), Binary to Bipolar Recoding (BBR).

**UNIT V ISSUES IN TIMING CLOSURE 9**

Static and Dynamic timing analysis, System Considerations - edge triggered, clock skew, handling asynchronous inputs, sequential machine, clock cycle time, Violation – maximum propagation delay, race through, Re-timings.

**Total 45 Hrs**

**h) Learning Resources**

**Text Books**


1. BehroozParhami, "Computer Arithmetic Algorithms and Hardware Designs", second edition, Oxford University Press, 2010
2. M. D. Ercegovac and T. Lang . "Digital Arithmetic", Elsevier Science (USA).2003


**Reference Books**


1. Ulrich W. Kulisch . "Advanced Arithmetic for the Digital Computer", Springer-Verlag

Wien, 2002.

**Online resources**

1. https://www.youtube.com/watch?v=iQHmtEtEggY