Course Code	Course Title	L	T	P	C
1152EC105	VLSI DESIGN TECHNIQUES	3	0	0	3

a) Course Category

Program Elective

b) Preamble

This course introduces basic techniques and algorithms for physical design and optimization of VLSI circuits. The necessary background in graph theory and mathematical optimization, application of different analytical and algorithmic techniques to physical design of VLSI circuitswill be studied. The students shall emphasize VLSI design issues encountered in deep submicron technology. Throughout the course, students will be exposed to research methodology and to a set of academic and commercial CAD tools for physical design.

c) Prerequisite

VLSI Design

d) Related Courses

Low Power VLSI Design, Analog VLSI Design

e) Course Outcome

Upon the successful completion of the course, students will be able to:

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Explain the design automation algorithms and various constraints posed by VLSI fabrication and design technology.	K2
CO2	Illustrate the layout optimization techniques and map them to the algorithms.	K2
CO3	Classify the design algorithms to meet the physical design parameters.	K2
CO4	Summarize VLSI interconnects and routing strategies in deep sub-micron.	K2

CO5	Restate sub-micron challenges and relate them to issues in physical synthesis of ICs.	K2

f) Correlation of COs with Pos

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	H	H	M	L	-	-	-	L	-	-	-	M	M	-
CO2	H	L	M	H	-	-	-	L	-	-	-	L	M	-
CO3	M	L	H	M	-	-	-	L	-	-	-	L	L	-
CO4	H	H	M	H	-	-	-	L	-	-	-	M	M	-
CO5	M	M	H	H	-	-	-	L	-	L	-	M	L	-

g) Course Content

UNIT I DESIGN METHODS AND AUTOMATION TOOLS 9

Design domains and Actions – Design methods and Technologies – Levels of abstractions in Design Automation tools – Graph terminology – data structures for the representation of graphs – Computational complexity – Graph Algorithms: Depth-First Search Algorithm, Breadth-First Search Algorithms and Dijikstra's Shortest path Algorithms.

UNIT II LAYOUT DESIGN 8

Design Rules – Symbolic Layout – Problem Formulation: Applications of compaction, Informal Problem formulation, Graph theoretical formulation, Maximum design constraints, Algorithms for Constraintgraph compaction.

UNIT III PLACEMENT, PARTITIONING AND PLANNING 10

Circuit Representation – Wire length estimation – Placement Problems – Placement Algorithms: Constructive placement, Iterative improvements – Partitioning: K-Lin Partitioning Algorithms - Floorplanning concepts: Terminology and Floorplan representation, Optimization problems in Floorplanning – Shape functions and Floorplan sizing.

UNIT IV ROUTING 9

Local routing problems – Area routing – Channel routing: Models, The vertical constraint graphs, horizontal constraints and left-edge algorithms, Channel Routing Algorithms – Global Routing: Standard cell layout, Building-block layout and Channel ordering, Algorithms for Global Routing: Problem definition and discussion, efficient rectilinear Steiner-Tree construction, Local transformations for Global Routing.

UNIT V SIMULATION, SYNTHESIS AND VERIFICATION 9

Gate level modelling: Signal Modelling, Gate modelling, Delay modelling, Connectivity modelling,

Compiler driven simulation, Event driven simulation – Switch level modelling: Connectivity and Signal Modelling, Simulation Mechanisms – Combinational logic synthesis, Binary Decision Diagrams, Two level logic synthesis.

Total 45 Hrs

h) Learning Resources

Text Books

1. Sabih H. Gerez, “Algorithms for VLSI Design Automation,” Wiley India Pvt Ltd, 2006.
2. Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation,” Springer, 2005.

Reference Books

1. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation,” CRC Press, 2008.
2. M. Sarrafzadeh and C.K. Wong, “An Introduction to VLSI Physical Design,” McGraw Hill, 1996.