Course Code	Course Title	L	T	P	C
1152EC103	SILICON VALIDATION	3	0	0	3

a) Course Category

Program Elective

b) Preamble

The purpose of this course is to know the basics of testing, test generation of combinational circuits, sequential circuits and design strategies for test and system level test.

c)Prerequisite

VLSI Design.

d) Related Courses

Low Power VLSI, Analog VLSI Design.

e) Course Outcomes

Upon the successful completion of the course, student will be able to:

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Explain the basics of Testing and Fault Modeling	K2
CO2	Illustrate the logical and fault simulation techniques.	K2
CO3	Classify the various test generation algorithms for sequential and combinational circuits.	K2
CO4	Summarize the design strategies for test, system level and memory test.	K2
CO5	Explain the concept of Built In Self Test for digital systems and its methodology.	K2

f) Correlation of COs with POs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	H	M	L	-	-	L	L	-	-	-	-	L	L	-

CO2	H	L	M	-	M	-	-	-	L	-	-	L	L	-
CO3	M	H	L	M	-	-	-	-	L	-	-	L	L	-
CO4	H	L	M	-	-	-	-	L	-	L	-	M	L	-
CO5	H	M	M	L	L	-	-	-	L	-	-	M	L	-

g) Course Content

UNIT I BASICS OF TESTING 9

Need for Testing,Testing at Various Levels, Objectives of Testing - VLSI Test process and Test Equipment - Types of Testing: Functionality Tests, Silicon Debug, Manufacturing Tests, Defect during manufacturing - Fault Modelling, Observability and Controllability, Fault Coverage, Fault Sampling - ATE, Test economics.

UNIT II LOGICAL AND FAULT SIMULATION 9

Simulation for design verification, Simulation for Test evaluation - logical and fault simulation, Characteristics of Fault Simulation, Classical Fault Simulation Techniques, Modern Fault Simulation for Combinational Circuits - Hardware Approaches to Fault Simulation.

UNIT III COMBINATIONAL AND SEQUENTIAL CIRCUITS TEST GENERATION 9

Combinational Circuits: Algorithms representations, Redundancy Identification (RID), Significant Combinational ATPG Algorithms, Test Generation, Test Compaction - Sequential Circuits: ATPG for single clock synchronous circuits, Time-Frame expansion method, Simulation based sequential circuits.

UNIT IV DESIGN STRATEGIES FOR TEST AND SYSTEM LEVEL TEST 9

Design for Testability, Ad hoc Testing, Scan Based Test Techniques, Memory Testing, IDDQ Testing, IDDQ testing Methods - Boundary Scan, Boundary Scan Architecture, Test Access Port (TAP), TAP Controller, Instruction Registers, Data Register, Boundary Scan Register, Bypass Register.

UNIT V BUILT IN SELF TEST 9

Buit In Self Test, Test Pattern Generation for BIST, Circular BIST, BIST Architectures - Testable Memory Design, Test Algorithms, Test Generation for Embedded RAMs, BIST for Delay Fault Testing.

Total 45 Hrs

h) Learning Resources

Text Books

1. Weste and Eshraghian, “Principles of CMOS VLSI design”, Pearson Education, 1999

2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2004

3. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002
4. N.K. Jha and S.G. Gupta, “Testing of Digital Systems”, Cambridge University Press, 2003

Reference Books

1. W. W. Wen, “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann
2. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.
3. ZainalabeNavabi, “Digital System Test and Testable Design: Using HDL Models and Architectures”, Springer, 2010
4. A.K Sharma, Semiconductor Memories Technology, Testing and Reliability, IEEE.
5. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House

Online Resources

1. www.nptel.ac.in/courses/106103016