Course Code	Course Title	L	T	P	C
1152EC102	LOW POWER VLSI DESIGN	3	0	0	3

a) Course Category

Program Elective

b) Preamble

This course provides the basic and design knowledge about low power VLSI which involvessources of power dissipation, power optimization techniques and power estimation

c) Prerequisite

VLSI Design

d) Related Courses

VLSI Design Techniques, Analog VLSI Design

e) Course Outcomes

On successful completion of this course the student will be able to

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Explain the sources of power dissipation in CMOS	K2
CO2	Classify the special techniques to mitigate the power consumption in VLSI circuits	K2
CO3	Summarize the power optimization and trade-off techniques in digital circuits.	K2
CO4	Illustrate the power estimation at logic and circuit level	K2
CO5	Explain the software design for low power in various level	K2

f) Correlation of Cos with POs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	H	H	M	L	-	-	-	-	-	-	-	H	M	-
CO2	H	L	M	H	-	-	-	-	-	-	-	L	H	-

CO3	M	L	H	M	-	-	-	-	-	-	-	L	L	-
CO4	H	H	M	H	-	-	-	-	-	-	-	M	M	-
CO5	M	M	H	H	-	-	-	-	-	-	-	H	L	-

h) Course Content

UNIT I POWER DISSIPATION IN CMOS 9

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET , gate induced drain leakage– Power dissipation in CMOS : short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design, hierarchy of limits, fundamental limit, material limit, device limit, system limit.

UNIT II POWER OPTIMIZATION USING SPECIAL TECHNIQUES 9

Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques - CMOS Floating Node: Tristate Keeper Circuit, Blocking Gate, Low Power Bus: Low Swing Bus, Charge Recycling Bus, Delay Balancing - Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Word line and Reduced bit line Swing

UNIT III DESIGN OF LOW POWER CIRCUITS 9

Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Combinational Flip-flop, Double Edge Triggered Flip-flop - Low Power Digital Cell Library : Cell Sizes and Spacing, Varieties of Boolean Functions, Adjustable Device Threshold Voltage

UNIT IV POWER ESTIMATION 9

Modelling of signals - signal probability calculation - Statistical techniques - estimation of glitching power-Sensitivity analysis-Power estimation using input vector compaction, power dissipation in Domino logic, circuit reliability, power estimation at the circuit level, Estimation of maximum power: test generation based approach, steepest descent, generic based algorithm based approach

UNIT V SOFTWARE DESIGN FOR LOW POWER 9

Sources of software power dissipation - software power estimation: Gate level, architecture level, bus switching activity, instruction level power analysis - software power optimization: minimizing memory access costs, instruction selection and ordering, power management - Automated low power code generation – Co-design for low power.

Total 45 Hrs

i) Learning Resources

Text Books

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998

Reference Books

1. DimitriosSoudris, Christians Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002
2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999
3. AbdelatifBelaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995
4. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001
5. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing

Online Resources

1. http://nptel.ac.in/syllabus/106105034/
2. https://www.youtube.com/watch?v=LjDb6VQlOeQ
3. http://freevideolectures.com/Course/3059/Low-Power-VLSI-Circuits-and-Systems
4. http://www.springer.com/us/book/9788132219361