Course Code	Course Title	L	T	P	C
1152EC133	DSP ALGORITHMS AND ARCHITECTURE	3	0	0	3

a) Course Category

Program Elective

b) Preamble

DSP algorithms and Architecture course provides an introduction on the industry based DSP processor's architecture and their algorithms. Students will learn about the addressing modes, instruction set and memory allocation of the TMS320C67XX processor.

c) Prerequisite

Discrete Time Signal Processing

d) Related Courses

Signal Processing for Speech Recognition

e) Course Outcome

Upon the successful completion of the course, student will be able to:

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Explain the basic constituents of a digital signal processor.	K2
CO2	Explain the architecture of TMS320C67XX processor.	K2
CO3	Demonstrate the basic DSP algorithms on TMS320C67XX processor.	K3
CO4	Describe the interfacing concepts of external memory, serial and parallel I/O devices.	K2
CO5	Identify the development tools and blocks involved in DSP applications.	K2

f) Correlation of COs with POs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	M	-	-	-	-	-	-	-	-	-	-	M	-	-

CO2	M	-	-	-	-	-	-	-	L	L	-	L	-	-
CO3	M	L	L	L	H	-	L	L	L	L	-	L	L	H
CO4	L	M	-	-	-	-	-	-	L	L	-	L	-	-
CO5	L	-	-	-	L	-	-	-	L	L	-	L	L	L

g) Course Content

UNIT I ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL PROCESSORS 9

Introduction: Basic Architectural Features – DSP Computational Building Blocks – Bus Architecture and Memory – Data Addressing Capabilities – Address Generation Unit – Programmability and Program Execution – Features for External Interfacing.

UNIT II PROGRAMMABLE DIGITAL SIGNAL PROCESSORS 9

Introduction, Commercial digital Signal processing Devices, TMS320C67XX Processor: Data Addressing Modes - Memory Space - Program Control - Detail Study of Instructions and Programming - On-Chip peripherals - Interrupts - Pipeline Operation.

UNIT III IMPLEMENTATION OF BASIC DSP ALGORITHMS 9

Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case), Implementation of FFT Algorithms: Overflow and Scaling – Bit Reversed Index Generation – Implementation on the TMS320C67XX.

UNIT IV INTERFACING MEMORY, SERIAL AND PARALLEL I/O PERIPHERALS TO DSP DEVICES 9

Introduction, Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA), Synchronous Serial Interface.

UNIT V DEVELOPMENT TOOLS AND APPLICATIONS OF DSP PROCESSOR9

DSP Development Tools – The DSP System Design Kit (DSK) – The Assembler and the Assembly Source File – The Linker and Memory Allocation – The Code Composer Studio. Building blocks involved in a DSP Based Bio-telemetry Receiver and Image Processing Algorithms.

Total 45 Hrs

h) Learning Resources

Text Books

1. Avtar Singh and S. Srinivasan, “Digital Signal Processing”, 4th edition, Thomson Publications, 2004
2. Sen M. Kuo, Woon-Seng S. Gan, “Digital Signal Processor-Architectures, implementation, and Applications”, pearson prentice hall, 2005 .

Reference Books

1. Peter Pirsch, “Architectures for Digital Signal Processing”, 2nd edition, John Weily, 2007
2. B. Venkataramani and M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications”, 2 Edition, TMH, 2004.
3. Jervis, “Digital Signal Processing- A practical approach”, 4th edition, Pearson Education,2004.
4. J.G.Proakis, “Algorithms for Statistical Signal Processing”, 4th edition, Pearson, 2002.
5. TMS320C50, TMS320C54XX, TMS320C6713 data books.

Online Resource

1. http://www.ti.com/product/TMS320C6713/technicaldocuments
2. http://www.ti.com/tool/tmdsdsk6713