Course Code	Course Title	L	T	P	C
1156EC408	VERIFICATION TESTBENCHES USING OVM AND UVM	0	0	0	2

a) Course Category

Independent Self Learning course

b) Preamble

The verification industry for VLSI Technology is adopting various languages including System Verilog based Universal Verification Methodology (UVM) at a rapid pace for most of the current ASIC/SOC Designs and is considered as an important skill for front end VLSI design/verification

c) Prerequisite

Nil

d) Related Courses

VLSI Design, Reconfigurable Computing with FPG

e) Course Outcomes

After the completion of this course, the students should be able to

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Understand the basic concepts of two methodologies - OVM and UVM	K2
CO2	Build actual testbenches based on UVM from grounds up.	K2
CO3	Generate sequence-based stimulus for VLSI frontend design.	K2
CO4	Code testbenches using UVM and OVM.	K2
CO5	Understand Advanced Peripheral Bus testbenches.	K2

f) Course Content

UNIT I INTRODUCTION

Need for Verification Methodologies, Layered Testbench Architecture, Introduction to OVM, UVM Concepts, Transaction Level Modelling Basics, TLM Interfaces

UNIT II BUILDING A TESTBENCH COMPONENT

Testbench Components and Hierarchy, Driver and Sequencer Components, Sequencer to Driver Connection, Monitor Component, Agent Component, Environment and Test Class Components, Environment and Test Class Components, Understanding Simulation phases.

UNIT III SEQUENCE BASED STIMULUS GENERATION

Basics of Sequence based Stimulus Generation, Sequence Items and Methods, Sequences and its Methods, Sequencer and Driver API, Sequence Generation Styles, Basics of Virtual Sequences

UNIT IV DYNAMIC CONSTRUCTIONS AND CONFIGURATIONS

Basic Concepts of OVM/UVM Factory, Testbench Configuration in UVM, Test Mechanisms in UVM

UNIT V ASSIGNMENT IN TESTBENCHES

Assignment, APB: Protocol, Testbench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.

g) Learning Resources

Reference Books

1. https://www.udemy.com/learn-ovm-uvm/
2. http://www.testbench.in/UT_00_INDEX.html
3. http://www.testbench.in/OT_00_INDEX.html