Course Code	Course Title	L	T	P	C
1156EC407	SYSTEM ON CHIP VERIFICATION USING SYSTEM VERILOG	0	0	0	2

a) Course Category

Independent Learning – Self Learning Course

b) Preamble

This course introduces the concepts of System on Chip Design Verification with emphasis on Functional Verification flows and methodologies. The course also teaches how to code in System Verilog language - which is the most popular Hardware Description Language used for SOC design and verification in semiconductor industry. The course is organised into multiple sections to practically code, simulate and verify using a free browser based Simulator and Waveform viewer

c) Prerequisite

VLSI Design

d) Related Courses

Verification Test Benches using OVM and UVM

Verification using System C

e) Course Outcomes

CO Nos.	Course Outcomes	Knowledge Level (Based on Revised Bloom's Taxonomy)
CO1	Explain theSOC, VLSI design flow, and overview of System Verilog	K2
CO2	Summarize the concepts of VLSI design verification flow and methodology.	K2
CO3	Code, simulate and verify System Verilog Test benches	K3
CO4	Explain the concepts of System Verilog OOPs and Randomization	K2
CO5	Make use of threads, and inter processor communication in System Verilog	K2

f) Course Content

UNIT I Introduction to SOC and System Verilog Language

Introduction to SOC, VLSI Design Flow, History and overview of System Verilog, Language construct- Data Types and operators, Loops, flow control, Task and functions, SV arrays – Queues, Coding of a design

UNIT II Verification basic and concepts

Functional Verification flows and methodologies, Verification - Planning approach - Metrics, Verification methodologies - Simulation- formal - assertion -directed vs constrained random verification and coverage, Hardware-software verification and Emulation

UNIT III Basic System Verilog Test Benches

Interfaces, Clocking Blocks, Program Blocks, Direct Program Interface, Coding interfaces and clocking blocks

UNIT IV System Verilog OOPs Concept and Randomization

Basic OOPs Concept, System Verilog Classes, Virtual Interfaces, Random Constraint and usage

UNIT V Threads and inter processor communication

Process and Threads in System Verilog, System Verilog Mailboxes, Synchronization –Event and semaphore, Connecting all TB components using Mailboxes, Built Top TB and compile etc

g) Learning Resources

Online Resources

1. https://verificationexcellence.usefedora.com/p/learn-systemverilog
2. https://www.design-reuse.com/articles/23742/systemverilog-verification-methodology.htm
3. http://www.asicguru.com/system-verilog/tutorial/introduction/1/