Agreement of Cooperation and Exchange
between
National Sun Yat-sen University, Taiwan
and
Vel Tech Rangarajan Dr.Sagunthala R&D Institute of Science and Technology (Deemed University), India

For the purpose of furthering cooperation in both education and academic research, National Sun Yat-sen University (hereinafter as NSYSU) and Vel Tech Rangarajan Dr.Sagunthala R&D Institute of Science and Technology (Deemed University) (hereinafter as Vel Tech) hereby affirm their intent to promote academic cooperation and exchange as well as mutual benefit to their respective universities. Academic cooperation and exchange are considered to include but are not limited to:

1. Exchange of faculty and students;
2. Exchange of data, documents, and research materials in fields of mutual interest;
3. Coordination such activities as joint research, lectures, and symposia.

The purpose of faculty exchange is to promote collaboration on research and academic resources, whereas the exchange of students aims at allowing students to enroll at the host university for academic credits that will be recognized by and applied toward their degrees at the home university.

Faculty Exchange

Both universities shall make efforts to encourage collaboration among faculty members. The host university shall provide as much as possible an office space and access to facilities for a visiting faculty. Unless otherwise agreed upon, the host university shall not be financially responsible for the expenses incurred by a concerned visiting faculty member during the exchange period.

Student Exchange

Both universities agree to accept and enroll exchange students as full-time students for the duration of their exchange programs. Both universities shall prepare a detailed program to provide the exchange students the educational resources, both administrative and academic, to allow the program to yield maximum benefit.

The home university shall encourage students to obtain health insurance coverage before joining their host university. However, it is the responsibility of the host university to assist exchange students in finding accommodation,

preferably on campus. Drawing into consideration the difference in academic calendars, both universities agree to make necessary arrangements for the incoming exchange students to allow them to earn credits and to fulfill the residency requirements of their respective home university.

Both universities will screen students, undergraduate and graduate, for high academic performance to participate in the exchange program. An equal number of students from each university will be exchanged during the term of this agreement. The period of stay for an exchange student will be for one or two semesters. Students who wish to participate in subject courses offered at the host university must satisfy the language proficiency requirements of the host university. Those who wish to enroll in language courses are required to submit an enrollment proposal to be approved by the home university. At the end of each academic term, the host university shall forward to the home university an official transcript of credits for each of the exchange students.

Exchange students will pay tuition at the home university. They are also financially responsible for all the expenses related to travel to and from the host university, accommodation and living, health insurance coverage, books and other miscellaneous items for the duration of their exchange program.

Period of Agreement

This agreement shall become effective from the date of signature and continue to be in force for five years. It can be extended for another five years upon mutual consent. Should either university wish to terminate the agreement before the expiry date, it shall notify in written form the other of its intention to terminate it at least six months before the date of its proposed termination.

Amendment

This agreement may be amended by mutual consent of the two universities.

In WITNESS WHEREOF, the parties have set their hands on the date and place mentioned below.

Prof. Ying-Yao Cheng
President
National Sun Yat-sen University

Date: 2019. 3. 22

Col. Prof. R Rangarajan
Founder Chancellor & President
Vel Tech

Date: 03 APR 2019

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

National Sun Yat-sen University, Taiwan

Name of the Research Institute/University/ Organization	Country	Duration of the Agreement	Academic Year	Date of Signing	Date of Expiry	Purpose/Activities
National Sun Yat-sen University	Taiwan	10 years	2018-19	03.04.2019	02.04.2029	Exchange of faculty and students; Exchange of data, documents, and research materials in fields of mutual interest; Coordination in activities such as joint research, lectures and symposia

Actual Activities with National Sun Yat-sen University, Taiwan	
A.Y. 2018-19	Faculty Mobility (Incoming - Short Courses) - 1
A.Y. 2019-20	Student Mobility (Outgoing-Project Work) - 4 Faculty Mobility (Incoming - Short Courses) - 1
A.Y. 2020-21	Discussed Potential Collaborative Activities via Virtual Meet (Research collaborations, Faculty & Student Mobility, Dual degree programs)

MoU Coordinator

Vel Tech * India * Office of International Relations *
19 FEB 2022

Dean - International Relations

Dr. P. Suresh
Dean -International Relations

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

School of Electrical & Communication

Department of Electronics & Communications Engineering

Specialized one credit course on

"Integrated Circuit Design using CMOS Technology"

(1157EC922)

by

Prof. Dr. Chua-Chin Wang

National Sun Yat-Sen University, Taiwan

國立中山大學
National Sun Yat-sen University

Held on

Date: March 30 to April 2, 2019

Chua-Chin Wang

Dept. of Electrical Engineering
National Sun Yat-Sen University
70, Lian-Hai Rd., Kaohsiung, Taiwan 80424
Tel : +886-7-5252000 ext. 4144
Fax : +886-75254199
Email : ccwang@ee.nsysu.edu.tw



EDUCATION :

07/1992	**Ph. D. in EE**, State University of New York (SUNY) at Stony Brook
07/1988	**M. S. in EE**, State University of New York (SUNY) at Stony Brook
06/1984	**B. S. in EE**, National Taiwan University (NTU)

EXPERIENCE :

Time	Position
08/2014-07/2017	**Dean**, College of Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan
08/2014-01/2015	Vice President, Office of Industrial Collaboration and Continuing Education Affairs, National Sun Yat-Sen University, Kaohsiung, Taiwan
08/2012-07/2014	**Chief Executive Officer,** Operation Center of University-Industry Cooperation, National Sun Yat-Sen University, Kaohsiung, Taiwan
01/2011-12/2015	**Principal Investigator**, Green Electronics Program of National Program of Intelligent Electronics (NPIE), Taiwan
08/2009-07/2012	**Chairman,** Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan
01/2009-12/2010	**Co-Director,** Program 2 – Advanced SoC Design Technology, National Program for System-on-Chip (NSoC), Taiwan
10/2007-07/2009	**Director**, “Engineering Technology Research and Promotion Center” (ETRPC), National Sun Yat-Sen University, Kaohsiung, Taiwan
02/2006-present	**Professor,** National Sun Yat-Sen University, Kaohsiung,

	Taiwan
02/2005-01/2006	**Executive Secretary,** Asuka Semiconductor Inc., Hsinchu, Taiwan
02/1998-01/2005	**Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan
08/1992-01/1998	**Associate Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan
09/1986-08/1987	**EE Patent Engineer,** Taiwan Patent and Law Office (TIPLO), Taipei, Taiwan

Brief of Experience :

08/2014-07/2017	**Dean**, College of Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as Dean of Engineering college to lead 7 departments and institutes, 150 faculties and staffs, 2800 students for advanced research in versatile engineering areas, including EE, CSE, mechanical engineering, environmental engineering, etc.
08/2014-01/2015	**Vice President,** Office of Industrial Collaboration and Continuing Education Affairs, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as VP to integrate Operation Center of University-Industry Cooperation and Office of Continuing Education Affairs and develop full-scale industry-academia collaboration. A total of 15 MUSD funding is attained.
08/2012-07/2014	**Chief Executive Officer,** Operation Center of University-Industry Cooperation, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as CEO of NSYSU to lead 486 faculties, and 18 staffs, to attain a total of 12 MUSD research funding from industry and government for the university.
01/2011-12/2015	**Principal Investigator**, Green Electronics Program of National Program of Intelligent Electronics (NPIE), Taiwan ■ Serve as principal investigator to supervise and coordinate many government offices, including MOE, MOEA, NSC to promote green electronics design and fabrication, where a total of 300 MUSD is included.
08/2009-07/2012	**Chairman,** Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as the department head to lead 42 faculties, 10 staffs, more than 500 undergraduates, and 400 graduates in research and teaching ■ Acting Director of Institute of Communications Engineering to coordinate the research in communication systems ■ Initiated and founded the SOC group at Dept. of EE, NSYSU, to coordinate the SOC research activities.

01/2009-12/2010	**Co-Director,** National Science and Technology Program for System-on-Chip (NSoC) ■ Serve as the co-director to supervise and instruct Program 2 of NSoC Program, i.e., Advanced SoC Design Technology, where over 15 MUSD/year is involved.
10/2007-07/2009	**Director**, "Engineering Technology Research and Promotion Center" (ETRPC) ■ Founded and became the first Director of "Engineering Technology Research and Promotion Center" (ETRPC) of NSYSU to coordinate the research task and resource for government funded joint research projects ■ **principal investigator to develop "Reliability Design and Testing Technology of Integrated Circuits" including mixed-voltage I/O buffer under a total of 730,000 USD grant sponsored by MOEA (Ministry of Economics Affairs)**
02/2006-date	**Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan ■ **developed a very wide range digital I/O cell (0.9 V ~ 5.0 V) under $300,000 grants sponsored by Himax, the 13th largest IC Design house in the world** ■ coordinated and initiated to develop FlexRay transceiver circuit design and fault-tolerant ECU for car-use intranet under a total of $150,00 USD NSC grant and $60,000 USD grant from Chanshan Institute of Science and Technology
02/2005-01/2006	**Executive Secretary,** Asuka Semiconductor Inc., Hsinchu, Taiwan ■ founded Asuka Semiconductor Inc. and lead the RD division as the CTO (Chief Technology Officer) T ■ The first palm-sized DVB-T TV in the world: The power dissipation, sensitivity, heat removal difficulties were all resolved to produce a handheld DVB-T TV, called "ARA", with a 3.5" LCD panel. The mobility of ARA is over 70 km/hr with a single tuner.
02/1998-01/2005	**Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan ■ developed low-power and high-speed 4-T SRAM structure using low-Vthn bitline drivers and high-Vthp latches, and SRAM using negative wordline drivers ■ principal investigator to develop wireless implantable micro-stimulator SOC under a total of $150,000 USD NHRI (National Health Research Institute) grant ■ co-investigated an implantable neuron cell stimulation and measurement ASIC under a total of $200,000 USD NSC grant
08/1992-01/1998	**Associate Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan ■ **established VLSI Design Lab. in Dept. EE of NSYSU and developed all of the IC design environment and testing suite in NSYSU** ■ co-investigated an x86-compatible CPU under a total of $5.0 M NSC joint grant and developed high-speed low-power 64-b/32-b integer divisor using a table-sharing algorithm

	■ developed an image processing algorithm for wafer scratch identification under a $15,000 USD grant sponsored by Philips Semiconductor. The algorithm has been implemented and used in the factory to reduce around $100K USD/month manufacturing cost.
09/1986-08/1987	**EE Patent Engineer,** Taiwan Patent and Law Office (TIPLO), Taipei, Taiwan ■ successfully filed more than 100 patent applications for well-known enterprises, including Toshiba, Sony, Mitsushita, Motorola, Hitachi, TI, etc., in the following areas : circuit design, power electronics, memory design, wireless communication, etc. ■ successfully filed several re-examination for claim infringe cases

PROFESSIONAL ACTIVITIES :

Editorships

- **Associate Editor**, IEEE Trans. on Circuits & Systems – I : Regular Papers (2010~2012)
- **Associate Editor**, IEEE Trans. on Circuits & Systems – II : Brief Papers (2010~2011)
- **Guest Editor**, IEEE Trans. on Circuits & Systems – I :Regular Papers (2009)
- **Associate Editor**, IEICE Trans. on Electronics (2008~date)
- **Associate Editor**, J. of Signal Processing Systems (2009~date)
- **Associate Editor**, International J. of VLSI Design (2007~2009)
- **Guest Editor,** International Journal of Electrical Engineering (2007~2008)

Conf./Symp./TC Chairmanships

- **General Chair**, 2007 VLSI Design/CAD Symp. (Aug. 7~ 10, 2007, more than 1000 attendees)
- **Technical Committee Chair**, IEEE CAS Society Nanoelectronics and Giga-scale Systems (NG) Technical Committee (2008~2009)
- **General Co-Chair,** 2010 IEEE Inter. Symp. on Next-generation Electronics (2010 ISNE)
- **Conference Chair,** 2011 IEEE International Conference on IC Design and Technology (2011 ICICDT)
- **General Chair,** 2012 IEEE Asia Pacific Conference on Circuits and Systems (2012 APCCAS)
- **General Chair,** 2015 Symposium on Engineering, Medicine, Biology Applications (2015 SEMBA)
- **General Chair**, 2017 Taiwan-Philippines Joint Workshop (2017 TPJW)

Committee Memberships

- **Technical Committee,** IEEE CAS Society Multimedia Systems and Applications (MSA) Technical Committee
- **Technical Committee,** IEEE CAS Society VLSI Systems and Applications (VSA) Technical Committee
- **Technical Committee,** IEEE CAS Society Nanoelectronics and Giga-scale Systems (NG) Technical Committee
- **Technical Committee,** IEEE CAS Society Biomedical Circuits and Systems (BioCAS) Technical Committee
- **Technical Program Committee,** IEEE 2007 TENCON
- **Technical Program Committee,** 2008 Inter. Symp. on VLSI Design, Automation and Test (VLSI-DAT)
- **Technical Program Committee,** 2008 The 15th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2008)
- **Technical Program Committee,** 2008 IEEE Biomedical Circuits and Systems

Conference (BioCAS)

- **Track Chair & Technical Program Committee,** 2009 International Conference on IC Design and Technology (ICICDT'09)
- **Track Chair & Technical Program Committee,** 2009 European Conference on Circuit Theory and Design (ECCTD'09)
- **Steering Committee,** The 3rd Intelligent Living Technology Conference, ILT 2008 (2008)
- **Local Organizing Committee,** 2009 IEEE Asian Solid-State Circuits Conference (2009 A-SSCC)
- **Track Co-Chair,** 2008 IEEE Inter. Symp. on Circuits and Systems (2008 ISCAS)
- **Track Chair,** 2009 IEEE Inter. Symp. on Circuits and Systems (2009 ISCAS), 2010 IEEE Inter. Symp. on Circuits and Systems (2010 ISCAS)
- **Technical Advisory Committee,** 2012 IEEE Inter. Symp. on Circuits and Systems (2012 ISCAS)
- **Steering Committee,** VLSI Design/CAD Symp. (2008~date)
- **Steering Committee**, IEEE Asia Pacific Conference on Circuits and Systems (2014~date)

IEEE Administrative Service

- **Chapter Chair**, IEEE Tainan Section Circuits and Systems (CAS) Chapter (2007~2008)
- **Chapter Chair**, IEEE Tainan Section Solid-State Circuits (SSC) Chapter (2007~2008)
- **Board of Director**, IEEE Tainan Section (2008~2011)
- **Chair of Membership Development**, IEEE Tainan Section (2010~2011)
- **Vice Chair**, IEEE Tainan Section (2012~2013)
- **Board of Director,** IEEE Tainan Section (2015~2018)

Administrative Responsibilities

- **Patent Examiner,** Taiwan Intellectual Property Office (TIPO) (1998 ~ 2004)
- **Program Director**, Green Circuits Program Director of National Program on Silicon-On-Chip (NSOC), Taiwan (2009~2010)
- **Board of Director**, Taiwan IC Design (TICD) Academic Society (2003 ~ 2005), (2008~2012)
- **Science & Technology Advisory Board,** The Executive Yuan, Taiwan (2002 ~ 2005)
- **Technology Advisory Committee,** R&D Loan Project of Industrial Development Bureau, Ministry of Economic Affairs, Taiwan (2005~2007, 2009)
- **Advisory Board,** National Chip Implementation Center, Taiwan (2007~2012)
- **Board of Director,** Kaohsiung Branch of Chinese Institute of Engineers (2007~2008)
- **Founding President**, Taiwan Institute of Electrical and Engineering (TIEEE),

(2008~2012)

- **Program Director,** SBIR (Small Business Innovation Research) Program of Kaohsiung City (2014~date)
- **Board of Director**, Taiwan IC Industry and Academia Research Alliance (2016~2018)
- **Program Consultant,** National Program of Intelligent Electronics (NPIE) Bridge Program (2016~2018)
- **Board of Director,** Chinese Institute of Electrical Engineering (2017~2018)

DOMESTIC AWARDS & RECOGNITION

- **Distinguished Young Engineer Award** of Chinese Institute of Engineers (1999)
- **NSC (National Science Council) Research Award**(1994 ~1999)
- **Distinguished Engineering Professor Award** of Chinese Institute of Engineers (2006)
- **Distinguished Engineer Award** of Chinese Institute of Electrical Engineers (2006)
- **First Prize Award** of 2005 National IC Design Contest (Full Custom IC Design Category) of Ministry of Education, Taiwan.
- **First Prize Award** of 2006 National IC Design Contest (Analog IC Design Category) of Ministry of Education, Taiwan.
- **Distinguished Electrical Engineering Professor Award** of Chinese Institute of Electrical Engineers (2007)
- **Distinguished Engineering Professor Award** of Chinese Institute of Engineers (2012)
- **Outstanding Research Award**, National Sun Yat-Sen University, Taiwan (2012)
- **Distinguished Professor,** National Sun Yat-Sen University, Taiwan (2010~2013)
- **Outstanding Industry-Academia Collaboration Award** (2005, 2009, 2013)
- **Chair Professor,** National Sun Yat-Sen University, Taiwan (2013)
- **Best Technology Transfer Center Award**, Taiwan NSC/MOST (2012-2014)
- **Outstanding Industry-Academia Collaboration Award** of Chinese Institute of Engineers (2015)
- **President Candidate of National Sun Yat-Sen University,** recommended by President Recruit Committee of National Sun Yat-Sen University, Taiwan (2016)

INTERNATIONAL AWARDS & RECOGNITION

- IEEE Senior Member (2004 ~)
- **Distinguished Lecturer Program (DLP) Speaker Elected** : IEEE CAS Society (2008)
- **Best Paper Award (Outstanding Paper Award)** 2008 IEEE Inter. Conf. on Consumer Electronics (ICCE 2008), paper title : A transceiver design for ECU nodes in FlexRay-based automotive communication systems
- **Best Paper Award (Gold Leaf Award),** 2011 IEEE Asia Pacific Conference on

Postgraduate Research in Microelectronics & Electronics (PrimeAsia), paper title : On-chip process and temperature compensation and self-adjusting slew rate control for output buffer

- **Best Paper Award,** 2017 IEEE Inter. Conf. on Integrated Circuit, Design, and Verification (ICDV 2017), paper title : 2xVDD 28-nm CMOS digital output buffer using low-Vth transistors for slew rate adjustment

- **Keynote Speaker,** 2013 IEEE Inter. Symp. on Next-generation Electronics (2013 ISNE)
- **Keynote Speaker,** 2018 Joint Conf. on Electrical power, Electronic, Communication, Control, Informatic Systems (EECCIS 2018)

- **Invited Speaker**, 2012 TSMC Technology Forum
- **Invited Speaker**, 2015 International Taiwan Global Technology and Industry Summit Forum

- **IET (IEE) Fellow** (2012~date)
- **IEET Accreditation Chair** (2015~date)
- **Project Examiner,** National Science Foundation, USA (2016)
- **Project Examiner,** Ministry of Science, Technology and Space, Israel (2016)

PATENTS :

- 151 granted patents (including 24 US patents, 16 China patents)

PUBLICATIONS :

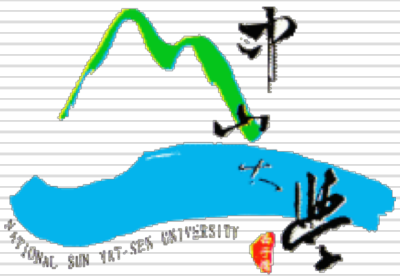
- 134 journal papers (including 60 IEEE journal/transaction papers), 269 conference papers, 2 book chapters

Integrated Circuit Design Using CMOS Technology

Chua-Chin Wang

Nov. 20, 2018

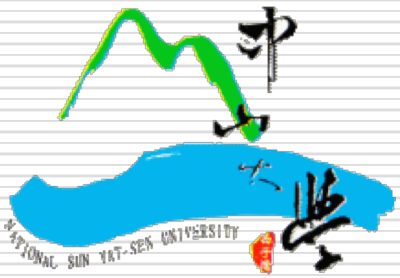
VLSI Design Laboratory
NSYSU-EE



Basic Topics



- Lecture 01: Introduction
- Lecture 02: Ratioless Logic Designs
- Lecture 03: Fabrication of CMOS Ics
- Lecture 04: Process integration
- Lecture 05: Layout Design Rules
- Lecture 06: Physical Layout Designs
- Lecture 07: RLC and Delay Models
- Lecture 08: Static Logic Circuits
- Lecture 09: Path-Delay Optimization
- Lecture 10: Dynamic Logic Circuits



Advanced Topics



Lecture 1 - 2 :

- Dynamic Analog Circuits & Nonlinear Analog Circuits
  - Switched-capacitor circuits, S/H, and filters
  - Comparator – data/bit slicing
  - Analog voltage multiplier

Lecture 3 - 4 :

- Data Converter (ADC & DAC)
  - Fundamentals, specs
  - Mixed-signal layout issues
  - Introduction of various architectures

Lecture 5 :

- Basics of Timing Circuit Designs
  - PLL
  - DLL
  - CDR

DINT/11-1
VT/ECE/201

Vel Tech

Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

Directorate of International Relations

Visiting Professor Programmes

Details of Professor & Course:

Name of the Professor	Prof. Dr. Chua-Chin Wang (CV Attached)
University & Country	National Sun Yat-Sen University , Taiwan
Title of the Course	Integrated Circuit Design using CMOS Technology
Department	Electronics and Communication Engineering
Dates of the Course	March 30 to April 2, 2019
Total No. of Hours	15
No. of Credits	1
Course Content	Attached

Prepared by:
Coordinator – Directorate of Intl. Relations

Forwarded by: 30/11/18
Director – Directorate of Intl. Relations

HoD

Dean 30/11/18

Director (Academic)

Vice Chancellor 5/12/2018

Dr.G.V.Uma
Prof. Dr.V.Jayasankar

Course code: 1157EC922

103

SNo	Stu_Id	Stu_Name	Stu_Degree	Stu_Branch	Stu_Test_SubjectCode	Stu_Test_SubjectName	Stu_Subject_PassFail	Stu_Grade
1	VtU7348	KAMBHAM PRAVEEN KUMAR REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
2	VtU7352	ATLA SRINIVAS	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
3	VtU7812	SHAIK SHABBER HUSSAIN	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
4	VtU5634	PRATEEK GOSWAMI	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
5	VTU6393	BALINENI HARIKRISHNA	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
6	VtU6591	BUJJA VIKAS	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
7	VTU6138	MANCHALA VENKATESHH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
8	VtU6557	MOHAMMED ASHIK K	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
9	VTU6144	NAGISETTYGARI KARTHIK	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
10	VTU6357	NAGOTHI PAVAN KUMAR	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
11	VTU6320	P RAM MANOHAR	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
12	VtU6623	SUJEET SINGH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
13	VtU6921	KRISHNARAO SANTHOSH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
14	VtU6933	MARAPELLY TEJA SAI	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
15	VtU7460	ROBIN JOSHUA R H	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
16	VtU7468	GUVVALA MANJULA	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
17	VtU7330	AVADHANAM VINDHYAVALI	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	RA
18	VtU8299	ANNALURI HARANADH KUMAR	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
19	VtU7479	VELISETY GANESH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
20	VtU7506	GURRALA SUMANTH BABU	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
21	VtU7910	BOGIREDDY MAHENDRA REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
22	VtU7421	KUPPAM AYYAVARU REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
23	VtU8083	MALE PRANEETHA REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
24	VtU8362	JINKA SURENDRA BABU	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	RA
25	VTU8535	KUMMARA PAVAN BHARGAV	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
26	VtU8088	BANDI HARSHITHA	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
27	VtU8165	GUTIGARI AYYAPPARAJU	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
28	VtU5836	VAIBHAV GIRI	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
29	VtU9706	PENAKATI MADHUSRI ANAND PADI NAIDU	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
30	VtU9745	MEDABALIMI AKASH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
31	VtU9259	NAGUMALLI SRINIVAS	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
32	VtU9286	BITRA BHANU NAGA SAI VAMSI	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	RA
33	VtU10159	MACHA BHARATH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
34	VtU8661	POKURI ANUDEEP REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
35	VtU8726	CHENNUPATI ABHINAV	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
36	VtU10070	KOPANATHI RAJENDRA PRASAD	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
37	VtU9047	THALAMADLA SANTHOSH KUMAR	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	RA
38	VtU9771	GUDE NANDHINI PRIYA	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
39	VtU9784	THOTA KRISHNA CHAITANYA	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	NE
40	VtU9792	INDLAMURI PHANDEENDRA VEERAYYA CHOWDARY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D

SNo	Stu_Id	Stu_Name	Stu_Degree	Stu_Branch	Stu_Test_SubjectCode	Stu_Test_SubjectName	Stu_Subject_PassFail	Stu_Grade
41	VtU9814	SATTI NAGA CHANDRA PRAKASH	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	RA
42	VtU9815	LEKKALA SIDDARTHA REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	RA
43	VtU9850	N.L.PRIYANKA	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
44	VtU9953	GUTLAPALLI MADHU SUDHANA RAO	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
45	VtU9958	MADI REDDY VISHNU VARDHAN REDDY	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	C
46	VtU9965	KAMASALA KIRAN KUMAR	B.Tech	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D
47	VtU8076	NARAYANA NELLURI VENKATESH	B.Tech	ECE(S.S)	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	D

VALID FOR 3 MONTHS ONLY FROM THE DATE OF ISSUE

विजया बैंक
VIJAYA BANK

वेलटेक इंजीनियरिंग कालेज शाखा, तमिलनाडु – 600062
VEL-TECH ENGINEERING COLLEGE, BRANCH, TAMILNADU - 600062
IFSC: VIJB0003802

A/c Payee

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Pay CHUA-CHIN WANG

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रूपये Rupees Fifty Two Thousand Four Hundred Twelve Only

अदा करें ₹ **52,412.00

A/c. No. 380206021000008

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INSTITUTE OF SCIENCE AND TECHNOLOGY

AUTHORIZED SIGNATORIES
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Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

Date: 26 MAR 2019

Our Ref. No: 2018-2019/VF158	**Your Ref. No:**

Name of the Professor: Prof. Dr. CHUA-CHIN WANG

University & Country : National Sun Yat-sen University, Taiwan

Course Title: Integrated Circuit Design using CMOS Technology

No. of Hours: 15

Department: Electronics and Communication Engineering

Program date: March 28- April 2, 2019

No. of Students: 35 (As per Vlearn)

Sl.No	Description	Amount in TWD	Amount in INR
1	Course Honorarium(15Hrs * INR 3000) Tax Free Net salary	20,092	45000
2	Visa Charges(3200NTD) 1 NTD= 2.3164 as on 16.03.2019	3200	7412
	Total	**23,292**	**52412**

(Rupees Fifty two thousand four hundred and twelve only)

In this regard, I request to transfer the amount in TWD to the following Account,

BANK NAME: BANK of TAIWAN

BRANCH NAME: KU SAN BRANCH

SWIFT CODE: BKTWTWTP051

BENEFICIARY's NAME: CHUA-CHIN WANG

BENEFICIARY's A/C: 051007027367

Thank You,

S. Sivaperumal

Dr. S. Sivaperumal
Director International Relations

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

No.42, Avadi - Vel Tech Road, Avadi,
Chennai, Tamil Nadu, Pincode - 600 062.
Toll Free: 1800 3070 6949
Landline: +91 44 2684 0262 / 2684 0605
Email : vtu@veltech.edu.in
Website: www.veltech.edu.in



विजया बैंक
VIJAYA BANK

वेलटेक इंजीनियरिंग कालेज शाखा, तमिलनाडु – 600062
VEL-TECH ENGINEERING COLLEGE, A/C Payee TAMILNADU - 600062
IFSC: VIJB0003802

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CHUA-CHIN WANG

Pay या धारक को or Bearer

Sixty Three Thousand Eight Hundred Seventy

रूपये Rupees

Seven Only

अदा करें ₹ **63,877.00

A/c. No. 380206021000008

VEL TECH RANGARAJAN DR. SAGUNTHALA R AND D
INSTITUTE OF SCIENCE AND TECHNOLOGY

AUTHORIZED SIGNATORIES

30/11/2018

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Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

Our Ref. No: 2018-2019/VF158	**Your Ref. No:**

Submitted for the Approval:

Name of the Professor: Prof. Dr. CHUA-CHIN WANG

University & Country : National Sun Yat-sen University, Taiwan

Course Title: Integrated Circuit Design using CMOS Technology

No. of Hours: 15

Department: Electronics and Communication Engineering

Program date: March 28- April 2, 2019

Sl.No	Description	Amount in TWD	Amount in INR
1	Flight ticket Reimbursement	28000	63877
	Total	**28000**	**63877**

(Rupees Sixty three thousand eight hundred and seventy seven only)

In this regard, Professor booked the ticket already. So I request your approval for transferring the amount in TWD to the following Account,

BANK NAME : BANK of TAIWAN

BRANCH NAME : KU SAN BRANCH

SWIFT CODE : BKTWTWTP051

BENEFICIARY's NAME : CHUA-CHIN WANG

BENEFICIARY's A/C : 051007027367

Rmb 4/1/2019

Thank You,

03/01/19.

S. Sivaperumal

Director
International Relations
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology * 1997 *

5/1

Entered in Budget Register
Pg. 24, Sl. 51
03/01/19.

National Sun Yat-sen University
Department of Electrical Engineering
Address: No. 70, Lienhai Rd.,
Kaohsiung 80424 Taiwan, R.O.C
https://web.ee.nsysu.edu.tw/

International Exchange Program

Student: K. Durga Srikanth from the department of Electronics and Communication Engineering in Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology has participated in the international exchange program administrated by the department of Electrical Engineering in National Sun Yat-sen University, Taiwan, for one semester (from September, 2019 to June, 2020), and completed the project, Design of 8-bit Carry Look Ahead Adder and Maximum Power Point Tracking of Photo Voltaic Module, in VLSI Design Laboratory.

Professor of VLSI Design Laboratory

Chairman of Electrical Engineering, NSYSU

July 9, 2020

National Sun Yat-sen University
Department of Electrical Engineering
Address: No. 70, Lienhai Rd.,
Kaohsiung 80424 Taiwan, R.O.C.
https://web.ee.nsysu.edu.tw/

International Exchange Program

Student: Shiva Reddy from the department of Electronics and Communication Engineering in Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology has participated in the international exchange program administrated by the department of Electrical Engineering in National Sun Yat-sen University, Taiwan, for one semester (from September, 2019 to June, 2020), and completed the project, Design of 8-bit Booth's Multiplier and Battery Management System (Broken Line Detection), in VLSI Design Laboratory.

Chua-Chin Wang Professor of VLSI Design Laboratory

Chih-Chiang Cheng Chairman of Electrical Engineering, NSYSU

July 9 2020

National Sun Yat-Sen University
Department of Electrical Engineering

National Sun Yat-sen University
Department of Electrical Engineering
Address: No. 70, Lienhai Rd.,
Kaohsiung 80424 Taiwan, R.O.C.
https://web.ee.nsysu.edu.tw/

International Exchange Program

Student: Dasari Venkatesh from the department of Electronics and Communication Engineering in Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology has participated in the international exchange program administrated by the department of Electrical Engineering in National Sun Yat-sen University, Taiwan, for one semester (from September, 2019 to June, 2020), and completed the project, Schematic Design of 1kBt SRAM and Layout Design of 1kB SRAM, in VLSI Design Laboratory.

Professor of VLSI Design Laboratory

Chairman of Electrical Engineering, NSYSU

July 9, 2020

National Sun Yat-Sen University Department of Electrical Engineering

National Sun Yat-sen University
Department of Electrical Engineering
Address: No. 70, Lienhai Rd.,
Kaohsiung 80424 Taiwan, R.O.C.
https://web.ee.nsysu.edu.tw/

International Exchange Program

Student: Akiri Jyoshnavi from the department of Electronics and Communication Engineering in Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology has participated in the international exchange program administrated by the department of Electrical Engineering in National Sun Yat-sen University, Taiwan, for one semester (from February, 2020 to June, 2020), and completed the project, Design of 8-bit Array Multiplier, in VLSI Design Laboratory.

Chua-Chin Wang, Professor of VLSI Design Laboratory

Chih-Chiang Cheng, Chairman of Electrical Engineering, NSYSU

July 9 2020

National Sun Yat-Sen University
Department of Electrical Engineering

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R&D Institute of Science and Technology
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School of Electrical and Communication

Department of Electronics and Communiction Engineering

Specialized one credit course on

"Full Custom Design of CMOS Logic Circuit"

(1157EC922)

by

Prof. Dr.Chua- Chin Wang

National Sun-Yat Sen University, Taiwan

國立中山大學
National Sun Yat-sen University

Held on

Date: March 2 to 6, 2020

Chua-Chin Wang

Dept. of Electrical Engineering
National Sun Yat-Sen University
70, Lian-Hai Rd., Kaohsiung, Taiwan 80424
Tel : +886-7-5252000 ext. 4144
Fax : +886-75254199
Email : ccwang@ee.nsysu.edu.tw



EDUCATION :

07/1992	**Ph. D. in EE**, State University of New York (SUNY) at Stony Brook
07/1988	**M. S. in EE**, State University of New York (SUNY) at Stony Brook
06/1984	**B. S. in EE**, National Taiwan University (NTU)

EXPERIENCE :

Time	Position
08/2014-07/2017	**Dean**, College of Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan
08/2014-01/2015	Vice President, Office of Industrial Collaboration and Continuing Education Affairs, National Sun Yat-Sen University, Kaohsiung, Taiwan
08/2012-07/2014	**Chief Executive Officer,** Operation Center of University-Industry Cooperation, National Sun Yat-Sen University, Kaohsiung, Taiwan
01/2011-12/2015	**Principal Investigator**, Green Electronics Program of National Program of Intelligent Electronics (NPIE), Taiwan
08/2009-07/2012	**Chairman,** Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan
01/2009-12/2010	**Co-Director,** Program 2 – Advanced SoC Design Technology, National Program for System-on-Chip (NSoC), Taiwan
10/2007-07/2009	**Director**, “Engineering Technology Research and Promotion Center” (ETRPC), National Sun Yat-Sen University, Kaohsiung, Taiwan
02/2006-present	**Professor,** National Sun Yat-Sen University, Kaohsiung,

	Taiwan
02/2005-01/2006	**Executive Secretary,** Asuka Semiconductor Inc., Hsinchu, Taiwan
02/1998-01/2005	**Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan
08/1992-01/1998	**Associate Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan
09/1986-08/1987	**EE Patent Engineer,** Taiwan Patent and Law Office (TIPLO), Taipei, Taiwan

Brief of Experience :

08/2014-07/2017	**Dean**, College of Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as Dean of Engineering college to lead 7 departments and institutes, 150 faculties and staffs, 2800 students for advanced research in versatile engineering areas, including EE, CSE, mechanical engineering, environmental engineering, etc.
08/2014-01/2015	**Vice President,** Office of Industrial Collaboration and Continuing Education Affairs, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as VP to integrate Operation Center of University-Industry Cooperation and Office of Continuing Education Affairs and develop full-scale industry-academia collaboration. A total of 15 MUSD funding is attained.
08/2012-07/2014	**Chief Executive Officer,** Operation Center of University-Industry Cooperation, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as CEO of NSYSU to lead 486 faculties, and 18 staffs, to attain a total of 12 MUSD research funding from industry and government for the university.
01/2011-12/2015	**Principal Investigator**, Green Electronics Program of National Program of Intelligent Electronics (NPIE), Taiwan ■ Serve as principal investigator to supervise and coordinate many government offices, including MOE, MOEA, NSC to promote green electronics design and fabrication, where a total of 300 MUSD is included.
08/2009-07/2012	**Chairman,** Dept. of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan ■ Serve as the department head to lead 42 faculties, 10 staffs, more than 500 undergraduates, and 400 graduates in research and teaching ■ Acting Director of Institute of Communications Engineering to coordinate the research in communication systems ■ Initiated and founded the SOC group at Dept. of EE, NSYSU, to coordinate the SOC research activities.

01/2009-12/2010	**Co-Director,** National Science and Technology Program for System-on-Chip (NSoC) ■ Serve as the co-director to supervise and instruct Program 2 of NSoC Program, i.e., Advanced SoC Design Technology, where over 15 MUSD/year is involved.
10/2007-07/2009	**Director**, "Engineering Technology Research and Promotion Center" (ETRPC) ■ Founded and became the first Director of "Engineering Technology Research and Promotion Center" (ETRPC) of NSYSU to coordinate the research task and resource for government funded joint research projects ■ **principal investigator to develop "Reliability Design and Testing Technology of Integrated Circuits" including mixed-voltage I/O buffer under a total of 730,000 USD grant sponsored by MOEA (Ministry of Economics Affairs)**
02/2006-date	**Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan ■ **developed a very wide range digital I/O cell (0.9 V ~ 5.0 V) under $300,000 grants sponsored by Himax, the 13th largest IC Design house in the world** ■ coordinated and initiated to develop FlexRay transceiver circuit design and fault-tolerant ECU for car-use intranet under a total of $150,00 USD NSC grant and $60,000 USD grant from Chanshan Institute of Science and Technology
02/2005-01/2006	**Executive Secretary,** Asuka Semiconductor Inc., Hsinchu, Taiwan ■ founded Asuka Semiconductor Inc. and lead the RD division as the CTO (Chief Technology Officer) T ■ The first palm-sized DVB-T TV in the world: The power dissipation, sensitivity, heat removal difficulties were all resolved to produce a handheld DVB-T TV, called "ARA", with a 3.5" LCD panel. The mobility of ARA is over 70 km/hr with a single tuner.
02/1998-01/2005	**Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan ■ developed low-power and high-speed 4-T SRAM structure using low-Vthn bitline drivers and high-Vthp latches, and SRAM using negative wordline drivers ■ principal investigator to develop wireless implantable micro-stimulator SOC under a total of $150,000 USD NHRI (National Health Research Institute) grant ■ co-investigated an implantable neuron cell stimulation and measurement ASIC under a total of $200,000 USD NSC grant
08/1992-01/1998	**Associate Professor,** National Sun Yat-Sen University, Kaohsiung, Taiwan ■ **established VLSI Design Lab. in Dept. EE of NSYSU and developed all of the IC design environment and testing suite in NSYSU** ■ co-investigated an x86-compatible CPU under a total of $5.0 M NSC joint grant and developed high-speed low-power 64-b/32-b integer divisor using a table-sharing algorithm

	■ developed an image processing algorithm for wafer scratch identification under a $15,000 USD grant sponsored by Philips Semiconductor. The algorithm has been implemented and used in the factory to reduce around $100K USD/month manufacturing cost.
09/1986-08/1987	**EE Patent Engineer,** Taiwan Patent and Law Office (TIPLO), Taipei, Taiwan ■ successfully filed more than 100 patent applications for well-known enterprises, including Toshiba, Sony, Mitsushita, Motorola, Hitachi, TI, etc., in the following areas : circuit design, power electronics, memory design, wireless communication, etc. ■ successfully filed several re-examination for claim infringe cases

PROFESSIONAL ACTIVITIES :

Editorships

- **Associate Editor**, IEEE Trans. on Circuits & Systems – I : Regular Papers (2010~2012)
- **Associate Editor**, IEEE Trans. on Circuits & Systems – II : Brief Papers (2010~2011)
- **Guest Editor**, IEEE Trans. on Circuits & Systems – I :Regular Papers (2009)
- **Associate Editor**, IEICE Trans. on Electronics (2008~date)
- **Associate Editor**, J. of Signal Processing Systems (2009~date)
- **Associate Editor**, International J. of VLSI Design (2007~2009)
- **Guest Editor,** International Journal of Electrical Engineering (2007~2008)

Conf./Symp./TC Chairmanships

- **General Chair**, 2007 VLSI Design/CAD Symp. (Aug. 7~ 10, 2007, more than 1000 attendees)
- **Technical Committee Chair**, IEEE CAS Society Nanoelectronics and Giga-scale Systems (NG) Technical Committee (2008~2009)
- **General Co-Chair,** 2010 IEEE Inter. Symp. on Next-generation Electronics (2010 ISNE)
- **Conference Chair,** 2011 IEEE International Conference on IC Design and Technology (2011 ICICDT)
- **General Chair,** 2012 IEEE Asia Pacific Conference on Circuits and Systems (2012 APCCAS)
- **General Chair,** 2015 Symposium on Engineering, Medicine, Biology Applications (2015 SEMBA)
- **General Chair**, 2017 Taiwan-Philippines Joint Workshop (2017 TPJW)

Committee Memberships

- **Technical Committee,** IEEE CAS Society Multimedia Systems and Applications (MSA) Technical Committee
- **Technical Committee,** IEEE CAS Society VLSI Systems and Applications (VSA) Technical Committee
- **Technical Committee,** IEEE CAS Society Nanoelectronics and Giga-scale Systems (NG) Technical Committee
- **Technical Committee,** IEEE CAS Society Biomedical Circuits and Systems (BioCAS) Technical Committee
- **Technical Program Committee,** IEEE 2007 TENCON
- **Technical Program Committee,** 2008 Inter. Symp. on VLSI Design, Automation and Test (VLSI-DAT)
- **Technical Program Committee,** 2008 The 15th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2008)
- **Technical Program Committee,** 2008 IEEE Biomedical Circuits and Systems

Conference (BioCAS)

- **Track Chair & Technical Program Committee,** 2009 International Conference on IC Design and Technology (ICICDT'09)
- **Track Chair & Technical Program Committee,** 2009 European Conference on Circuit Theory and Design (ECCTD'09)
- **Steering Committee,** The 3rd Intelligent Living Technology Conference, ILT 2008 (2008)
- **Local Organizing Committee,** 2009 IEEE Asian Solid-State Circuits Conference (2009 A-SSCC)
- **Track Co-Chair,** 2008 IEEE Inter. Symp. on Circuits and Systems (2008 ISCAS)
- **Track Chair,** 2009 IEEE Inter. Symp. on Circuits and Systems (2009 ISCAS), 2010 IEEE Inter. Symp. on Circuits and Systems (2010 ISCAS)
- **Technical Advisory Committee,** 2012 IEEE Inter. Symp. on Circuits and Systems (2012 ISCAS)
- **Steering Committee,** VLSI Design/CAD Symp. (2008~date)
- **Steering Committee**, IEEE Asia Pacific Conference on Circuits and Systems (2014~date)

IEEE Administrative Service

- **Chapter Chair**, IEEE Tainan Section Circuits and Systems (CAS) Chapter (2007~2008)
- **Chapter Chair**, IEEE Tainan Section Solid-State Circuits (SSC) Chapter (2007~2008)
- **Board of Director**, IEEE Tainan Section (2008~2011)
- **Chair of Membership Development**, IEEE Tainan Section (2010~2011)
- **Vice Chair**, IEEE Tainan Section (2012~2013)
- **Board of Director,** IEEE Tainan Section (2015~2018)

Administrative Responsibilities

- **Patent Examiner,** Taiwan Intellectual Property Office (TIPO) (1998 ~ 2004)
- **Program Director**, Green Circuits Program Director of National Program on Silicon-On-Chip (NSOC), Taiwan (2009~2010)
- **Board of Director**, Taiwan IC Design (TICD) Academic Society (2003 ~ 2005), (2008~2012)
- **Science & Technology Advisory Board,** The Executive Yuan, Taiwan (2002 ~ 2005)
- **Technology Advisory Committee,** R&D Loan Project of Industrial Development Bureau, Ministry of Economic Affairs, Taiwan (2005~2007, 2009)
- **Advisory Board,** National Chip Implementation Center, Taiwan (2007~2012)
- **Board of Director,** Kaohsiung Branch of Chinese Institute of Engineers (2007~2008)
- **Founding President**, Taiwan Institute of Electrical and Engineering (TIEEE),

(2008~2012)

- **Program Director,** SBIR (Small Business Innovation Research) Program of Kaohsiung City (2014~date)
- **Board of Director**, Taiwan IC Industry and Academia Research Alliance (2016~2018)
- **Program Consultant,** National Program of Intelligent Electronics (NPIE) Bridge Program (2016~2018)
- **Board of Director,** Chinese Institute of Electrical Engineering (2017~2018)

DOMESTIC AWARDS & RECOGNITION

- **Distinguished Young Engineer Award** of Chinese Institute of Engineers (1999)
- **NSC (National Science Council) Research Award**(1994 ~1999)
- **Distinguished Engineering Professor Award** of Chinese Institute of Engineers (2006)
- **Distinguished Engineer Award** of Chinese Institute of Electrical Engineers (2006)
- **First Prize Award** of 2005 National IC Design Contest (Full Custom IC Design Category) of Ministry of Education, Taiwan.
- **First Prize Award** of 2006 National IC Design Contest (Analog IC Design Category) of Ministry of Education, Taiwan.
- **Distinguished Electrical Engineering Professor Award** of Chinese Institute of Electrical Engineers (2007)
- **Distinguished Engineering Professor Award** of Chinese Institute of Engineers (2012)
- **Outstanding Research Award**, National Sun Yat-Sen University, Taiwan (2012)
- **Distinguished Professor,** National Sun Yat-Sen University, Taiwan (2010~2013)
- **Outstanding Industry-Academia Collaboration Award** (2005, 2009, 2013)
- **Chair Professor,** National Sun Yat-Sen University, Taiwan (2013)
- **Best Technology Transfer Center Award**, Taiwan NSC/MOST (2012-2014)
- **Outstanding Industry-Academia Collaboration Award** of Chinese Institute of Engineers (2015)
- **President Candidate of National Sun Yat-Sen University,** recommended by President Recruit Committee of National Sun Yat-Sen University, Taiwan (2016)

INTERNATIONAL AWARDS & RECOGNITION

- IEEE Senior Member (2004 ~)
- **Distinguished Lecturer Program (DLP) Speaker Elected** : IEEE CAS Society (2008)
- **Best Paper Award (Outstanding Paper Award)** 2008 IEEE Inter. Conf. on Consumer Electronics (ICCE 2008), paper title : A transceiver design for ECU nodes in FlexRay-based automotive communication systems
- **Best Paper Award (Gold Leaf Award),** 2011 IEEE Asia Pacific Conference on

Postgraduate Research in Microelectronics & Electronics (PrimeAsia), paper title : On-chip process and temperature compensation and self-adjusting slew rate control for output buffer

- **Best Paper Award,** 2017 IEEE Inter. Conf. on Integrated Circuit, Design, and Verification (ICDV 2017), paper title : 2xVDD 28-nm CMOS digital output buffer using low-Vth transistors for slew rate adjustment

- **Keynote Speaker,** 2013 IEEE Inter. Symp. on Next-generation Electronics (2013 ISNE)
- **Keynote Speaker,** 2018 Joint Conf. on Electrical power, Electronic, Communication, Control, Informatic Systems (EECCIS 2018)

- **Invited Speaker**, 2012 TSMC Technology Forum
- **Invited Speaker**, 2015 International Taiwan Global Technology and Industry Summit Forum

- **IET (IEE) Fellow** (2012~date)
- **IEET Accreditation Chair** (2015~date)
- **Project Examiner,** National Science Foundation, USA (2016)
- **Project Examiner,** Ministry of Science, Technology and Space, Israel (2016)

PATENTS :

- 151 granted patents (including 24 US patents, 16 China patents)

PUBLICATIONS :

- 134 journal papers (including 60 IEEE journal/transaction papers), 269 conference papers, 2 book chapters

Full Custom Design For CMOS Logic Circuit

Chua-Chin Wang

VLSI Design Laboratory
NSYSU-EE

Outlines of Lectures

- Introduction of IC Design Flows
  - cell-based, full-custom, FPGA
  - related EDA tools
- CMOS Digital Logic Circuits and Fabrication
  - CMOS circuits of Inverter (INV), NAND, NOR
  - Fabrication, Design Rules
  - Layouts of INV, NAND, NOR gates
  - Circuits of Latch and Flip-Flop
- Fundamental Logic Circuit Design Flow
  - dataflow, behavioral, structural levels
  - SPICE, layout, and simulation

Outlines of Hand-on Lab.

- HSPICE Circuit Simulation of INV, NAND, NOR
  - measuring critical path delay based on 0.18/0.35 um CMOS process
  - AC, DC, transient simulations
- Layout of INV, NAND, and NOR
  - DRC, LVS, LPE
- Pre-layout and post-layout simulations
  - All-PVT-corner simulations
  - debug
- 8-bit sub-system project
  - Adder, multiplier, or shifter
  - Unit cells and integration

Possible Dates for the Course

- 7 weekdays (not including Sat. and Sun.)

	Day 1	Day 2	Day 3	Day 4	Day 5	Day 6	Day 7
Morning Lecture Session (3 hrs)	Intro. of Digital IC Design	Combinational logic design	Sequential logic design	Memory design	Sub-system design	Mini-project design examples	Final Lecture Exam.
Afternoon Lab. Session (4 hrs)	Linux and Cadence S/W usage, schematic entry	Symbol view, HSPICE S/W usage	Logic gate, DFF design practice	Pre-layout timing, AC, DC, power simulation	Layout entry, post-layout simulation	Pad framing, stream out GDS-II	Final Lab. Exam. and mini-project practice
Note							

DINT/09-19/031

DA/13457
04/10/19.

UC/1158.

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R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

Details of Professor & Course:

Name of the Professor	Prof. Dr. Chua- Chin Wang (CV Attached)
University & Country	National Sun- Yat Sen University, Taiwan
Title of the Course	Full Custom Design for CMOS Logic Circuit
Department	Electronics and Communication Engineering
Dates of the Course	February 17 to 28, 2020 (7 working days) (7 hour/day.)
Total No. of Hours	45
No. of Credits	~~3~~ 2 credits
Category	Programme Elective
Course Content	Attached

Prepared by: 18/9/19

Coordinator – Directorate of Intl. Relations

Forwarded by: 18/09/19

Director – Directorate of Intl. Relations

HoD

Dean

Director (Academic)

Prof. Dr. techn. Koteswara Rao Anne
Director Academics

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology

Vice Chancellor

Prof. V. S. S. Kumar
Vice Chancellor

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

SNo	Stu_Id	Stu_Name	Stu_Branch	Stu_Test_Sub	Stu_Test_SubjectName	Stu_Subjec	Stu_Registrati	Stu_Exam	Stu_Gr
1	VtU7348	KAMBHAM PRAVEEN KUMAR REDDY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0111	6	C
2	VtU7352	ATLA SRINIVAS	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0005	6	D
3	VtU7812	SHAIK SHABBER HUSSAIN	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0238	6	D
4	VtU5634	PRATEEK GOSWAMI	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	14UEEC0139	8	D
5	VTU6393	BALINENI HARIKRISHNA	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0015	8	D
6	VtU6591	BUJJA VIKAS	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0024	8	C
7	VTU6138	MANCHALA VENKATESHH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0078	8	D
8	VtU6557	MOHAMMED ASHIK K	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0082	8	C
9	VTU6144	NAGISETTYGARI KARTHIK	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0088	8	D
10	VTU6357	NAGOTHI PAVAN KUMAR	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0089	8	D
11	VTU6320	P RAM MANOHAR	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	15UEEC0107	8	C
12	VtU6623	SUJEET SINGH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	15UEEC0121	8	NE
13	VtU6921	KRISHNARAO SANTHOSH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0284	6	D
14	VtU6933	MARAPELLY TEJA SAI	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0286	6	C
15	VtU7460	ROBIN JOSHUA R H	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0204	6	C
16	VtU7468	GUVVALA MANJULA	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0062	6	D
17	VtU7330	AVADHANAM VINDHYAVALI	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	16UEEC0006	6	RA
18	VtU8299	ANNALURI HARANADH KUMAR	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0082	6	D
19	VtU7479	VELISETY GANESH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	16UEEC0260	6	NE
20	VtU7506	GURRALA SUMANTH BABU	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0066	6	D
21	VtU7910	BOGIREDDY MAHENDRA REDDY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0022	6	D
22	VtU7421	KUPPAM AYYAVARU REDDY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0126	6	D
23	VtU8083	MALE PRANEETHA REDDY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0146	6	D
24	VtU8362	JINKA SURENDRA BABU	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	16UEEC0088	6	RA
25	VTU8535	KUMMARA PAVAN BHARGAV	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0502	6	D
26	VtU8088	BANDI HARSHITHA	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEEC0019	6	D
27	VtU8165	GUTIGARI AYYAPPARAJU	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	16UEEC0081	6	NE
28	VtU5836	VAIBHAV GIRI	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	14UEEC0184	8	D
29	VtU9706	PENAKATI MADHUSRI ANAND PADI N	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	17UEEC0365	4	NE
30	VtU9745	MEDABALIMI AKASH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0290	4	C
31	VtU9259	NAGUMALLI SRINIVAS	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0322	4	D
32	VtU9286	BITRA BHANU NAGA SAI VAMSI	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	17UEEC0054	4	RA

33	VtU10159	MACHA BHARATH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	17UEEC0259	4	NE
34	VtU8661	POKURI ANUDEEP REDDY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	17UEEC0376	4	NE
35	VtU8726	CHENNUPATI ABHINAV	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	17UEEC0082	4	NE
36	VtU10070	KOPANATHI RAJENDRA PRASAD	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	17UEEC0222	4	NE
37	VtU9047	THALAMADLA SANTHOSH KUMAR	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	17UEEC0478	4	RA
38	VtU9771	GUDE NANDHINI PRIYA	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0149	4	C
39	VtU9784	THOTA KRISHNA CHAITANYA	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	NE	17UEEC0481	4	NE
40	VtU9792	INDLAMURI PHANDEENDRA VEERAYY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0160	4	D
41	VtU9814	SATTI NAGA CHANDRA PRAKASH	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	17UEEC0424	4	RA
42	VtU9815	LEKKALA SIDDARTHA REDDY	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	RA	17UEEC0250	4	RA
43	VtU9850	N.L.PRIYANKA	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0323	4	C
44	VtU9953	GUTLAPALLI MADHU SUDHANA RAO	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0155	4	C
45	VtU9958	MADI REDDY VISHNU VARDHAN REDI	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0268	4	C
46	VtU9965	KAMASALA KIRAN KUMAR	ECE	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	17UEEC0187	4	D
47	VtU8076	NARAYANA NELLURI VENKATESH	ECE(S.S)	1157EC922	Integrated Circuit Design using CMOS Technology	Pass	16UEES0003	6	D

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Our Ref. No: 2019-2020/VF194	**Your Ref. No**:

Submitted for the Approval:

Name of the Professor: Prof. Dr. CHUA-CHIN WANG

University & Country : National Sun Yat-sen University, Taiwan

Course Title: Full custom Design for CMOS Logic Circuit

No. of Hours: 30

Category: Programme Elective

Department: Electronics and Communication Engineering

Program date: February 17 to 28, 2019

Sl.No	Description	Amount in TWD	Amount in INR
1	Flight ticket Reimbursement (1 TWD = 2.3482 as on 08.11.2019)	28000	65749
	Total	**28000**	**65749**

(Rupees Sixty five thousand seven hundred and forty nine only)

In this regard, Professor booked the ticket already. So I request your approval for transferring the amount in TWD to the following Account,

BANK NAME : BANK of TAIWAN

BRANCH NAME : KU SAN BRANCH

SWIFT CODE : BKTWTWTP051

BENEFICIARY's NAME : CHUA-CHIN WANG

BENEFICIARY's A/C : 051007027367

Thank You

21/11/19.

S. Sivaperumal

Entered in Budget Register

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21/11/19.

Delegates Attended in Virtual Meeting:

1. Prof. Chih-Wen Kuo, Vice President for International Affairs / Professor, Institute of Communications Engineering
2. Prof. Chua-Chin Wang, Professor, Department of Electrical Engineering
3. Ms. Tanya Hsu, Director, Division of International Relations, Office of International Affairs
4. Ms. Hana Ting, Program Coordinator, Division of Student Exchange, Office of International Affairs

University & Country : National Sun Yat-sen University, Taiwan

Date : 24.02.2021

Purpose: Discussed Potential Collaborative Activities via Virtual Meet

(Research collaborations, Faculty & Student Mobility, Dual degree programs)

